ABSTRACT OF THE DISCLOSURE

Techniques for forming devices, such as transistors, having vertical junction edges. More specifically, shallow trenches are formed in a substrate and filled with an oxide. Cavities may be formed in the oxide and filled with a conductive material, such a heavily doped polysilicon. Vertical junctions are formed between the polysilicon and the exposed substrate at the trench edges such that during a thermal cycle, the heavily doped polysilicon will out-diffuse doping elements into the adjacent single crystal silicon advantageously forming a diode extension having desirable properties.